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EXAMINER	
TORRES, JUAN A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,803	CHANG ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08-29-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The modifications to the drawings were received on 11/28/2005. These modifications are accepted by the Examiner.

Specification

The modifications to the specification were received on 11/28/2005. These modifications are accepted by the Examiner.

In view of the amendment filed on 11/18/2005, the Examiner withdraws the specification objections of the previous Office action.

The disclosure is objected to because of the following informalities: In the modifications to the specification, on page 11 in line 6 of the paragraph beginning at line 11, the recitation "Hands Fee I/F 338" is improper; it is suggested to be changed to "Hands Free I/F 338" (see figure 3).

Appropriate correction is required.

Claim Objections

In view of the amendment filed on 11/28/2005, the Examiner withdraws the claim objections to claims 8 and 23 of the previous Office action.

Response to Arguments

Applicant's arguments filed on 11/09/2005 have been fully considered but they are not persuasive.

Regarding claim 1 anticipated by Pukkila:

The Applicant contends, "The Office Action equates block 203 of Pukkila (Ampl., A/D) with the baseband processor of claim 16. Block 203 of Pukkila is a combined amplifier and analog to digital converter. A combined amplifier and analog to digital converter is simply not equivalent to a baseband processor. A baseband processor, in addition to performing amplification and analog-to-digital conversion operations, is capable of performing significant other baseband processing operations, as is described in the specification of the present application. Thus, the combine amplifier and analog to digital converter of Pukkila block 203 does not identically set forth the baseband processor of claim 1".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, the baseband processor claimed in claim 16 is "operable to receive analog signals corresponding to a data block and to produce samples of the analog signals". This is an A/D converter, if the baseband processor is doing more things those thing should be claimed. Pukkila is discloses in FIG. 2 a system operable to receive analog signals corresponding to a data block and to produce samples of the analog signals (figure 2 block 203 and figure 3 block 301 paragraphs [0024]-[0025] and [0027]).

The Applicant contends, "The Office Action equates three elements of claim 1 with block 205' of Pukkila. Firstly, the Office Action equates the equalizer of claim 1 with block 205 (of block 205') of FIG. 2 of Pukkila. Secondly, the Office Action equates the system processor with block 205' of FIG. 2 and operations of FIG. 3) of Pukkila. Thirdly,. the Office Action equates the IR processing module registers with block 205' of FIG. 2

and operations of FIG. 3) of Pukkila. Equating block 205' with multiple claim elements is impermissible in making an anticipation rejection. Each teaching of a prior art reference can only be used to meet one claim element. Because block 205' is cited against multiple elements of claim 1, Pukkila does not anticipate claim 1".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Block 205' includes a plurality of modules performing these operations.

The Applicant contends, "Block 205' is not a "system processor that is operable to receive the soft decision bits and to initiate IR operations" as required by claim 1".... "an IR processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits." Thus, Pukkila does not disclose either the system processor or the IR processing module of claim 1. For this reason, Pukkila does not anticipate claim 1.

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Pukkila discloses a system processor that is operable to receive the soft decision bits and to initiate IR operations (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]); and an IR processing module coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]).

The Applicant contends, "Pukkila further fails to describe the interaction among the elements of claim 1."

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Pukkila discloses a method and a system for performing Incremental Redundancy (IR) operations in a wireless receiver (FIGs. 2 and 3) comprising receiving an analog signal corresponding to a data block (figure 2 block 201 and figure 3 block 301 paragraphs [0024] and [0027]); sampling the analog signal to produce samples (figure 2 block 203 and figure 3 block 301 paragraphs [0024]-[0025] and [0027]); equalizing the samples to produce soft decision bits of the data block (figure 2 block 205 and figure 3 block 306 paragraphs [0025] and [0028]-[0029] and [0035]); configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]); initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]); and accessing, by the IR processing module, the plurality of IR processing module registers (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]); and performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031] and [0035]).

For these reasons and the reasons indicated in the previous Office Action the rejections of claim 1 is maintained.

Regarding claim 14 anticipated by Pukkila:

The Applicant contends, "The Office Action equates multiple elements of independent claim 14 with block 205' of FIG. 2 (blocks 305-318 of FIG. 3 of Pukkila. Firstly, the Office Action equates "at least one processing device" of claim 1 with block 205' of FIG. 2 and FIG. 3 blocks 305-318 of Pukkila. Secondly, the Office action equates "an IR processing module" of claim 1 with block 205' of FIG. 2 and FIG. 3 blocks 305-318 of Pukkila. Because block 205' is cited against multiple elements of claim 14, Pukkila does not anticipate claim 14.

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Block 205' includes a plurality of modules performing these operations.

The Applicant contends, "Block 205' is not "an IR processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits" as claim 14 requires. Thus, Pukkila does not disclose the IR processing module of claim 14. For this reason, Pukkila does not anticipate claim 14".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Pukkila discloses an IR processing module coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]).

The Applicant contends, "Pukkila further fails to disclose a processing device that initiates IR operations. While Pukkila discloses a method for performing IR operations, it fails to describe what structure of FIG. 2 could "initiate IR operations".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Pukkila discloses a system processor that is operable to receive the soft decision bits and to initiate IR operations (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]). The IR operations are initiated at block 306 of FIG. 3.

The Applicant contends, "Pukkila fails to "identically set forth" all elements of claim 14 and, for this reason, Pukkila fails to anticipate independent claim 14.

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Pukkila discloses a system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising a baseband processor that is operable to receive analog signals corresponding to a data block and to sample the analog signal to produce samples (figure 2 block 203 and figure 3 block 301 paragraphs [0024]-[0025] and [0027]); an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block (figure 2 block 205 and figure 3 block 306 paragraphs [0025] and [0028]-[0029]); a system processor that is operable to receive the soft decision bits and to initiate IR operations (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]); and an IR processing module coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]).

For these reasons and the reasons indicated in the previous Office Action the rejections of claim 14 is maintained.

Regarding Claims 1-3, 5, 8-16, 21-27, 30-32 and 34 anticipated by Parolari

The Applicant contends, "Parolari is not prior art under 35 U.S.C. 102(e)".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Parolari is continuation of PCT/EP02/03881, published in English with publication number WO 02/091655 on November 14, 2002 (included in this Office action), prior to the effective date of the present application. Also Parolari claims priority of the European patent application 1830283, published as EP 1255368 on November 11, 2002 (included in this Office action), also prior to the effective date of the present application. For these reasons and the reasons indicated in the previous Office action the rejections of claims 1-3, 5, 8-16, 21-27, 30-32 and 34 regarding Parolari are maintained.

Regarding Claims 4, 6, 17, 19, 20, 28, 29 and 33 anticipated by Parolari

The Applicant contends, "Parolari is not prior art under 35 U.S.C. 102(e)".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Parolari is continuation of PCT/EP02/03881, published in English, with US designation with publication number WO 02/091655 on November 14, 2002 (included in this Office action), prior to the effective date of the present application. Also Parolari claims priority of the European patent application 1830283, published as EP 1255368 on November 11, 2002 (included in this Office action), also prior to the effective date of the present application. For these reasons and the reasons indicated in the previous Office action the rejections of claims 4, 6, 17, 19, 20, 28, 29 and 33 regarding Parolari are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pukkila (US 20010017904 A1).

As per claim 1 Pukkila discloses a system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising a baseband processor that is operable to receive analog signals corresponding to a data block and to sample the analog signal to produce samples (figure 2 block 203 and figure 3 block 301 paragraphs [0024]-[0025] and [0027]); an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block (figure 2 block 205 and figure 3 block 306 paragraphs [0025] and [0028]-[0029]); a system processor that is operable to receive the soft decision bits and to initiate IR operations (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]); and an IR processing module coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations

on the soft decision bits (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031]).

As per claim 14 Pukkila discloses a system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising at least one processing device that is operable to receive an analog signal corresponding to a data block, to sample the analog signal to produce samples, to equalize the samples, to produce soft decision bits of the data block, and to initiate IR operations (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031] and [0035]); and an IR processing module coupled to the at least one processing device that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits (figure 2 block 205' and figure 3 blocks 305-318 paragraphs [0024]-[0031] and [0035]).

Claims 1-3, 5, 8-16, 18, 21-27, 30-32 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Parolari (US 20040081248 A1).

As per claim 1 Parolari discloses a system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising a baseband processor that is operable to receive analog signals corresponding to a data block and to sample the analog signal to produce samples (figure 5 block A/D paragraph [0112]); an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block (figure 5 block MLSE paragraph [0112]); a system processor that is operable to receive the soft decision bits and to initiate IR operations (figure 5 block channel decoder, control processor and incremental redundancy buffer paragraph [0112]); and an IR processing

module coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits (figure 5 block channel decoder, control processor and incremental redundancy buffer paragraph [0112]).

As per claim 2 Parolari discloses claim 1. Parolari also discloses that the system processor is operable to decode the soft decision bits to produce a decoded header for the data block (paragraphs [0024]-[0026]; paragraph [0074]; figure 4 and figure 5 paragraphs [0011] and [0112]).

As per claim 3 Parolari discloses claim 1. Parolari also discloses that the IR processing module is operable to decode the soft decision bits to produce a decoded header for the data block (paragraphs [0024]-[0026]; paragraph [0074]; figure 4 and figure 5 paragraphs [0011] and [0112]).

As per claim 5 Parolari discloses claim 1. Parolari also discloses that when the IR operations are unsuccessful, the soft decision bits of the data block are stored in IR memory (figure 5 incremental redundancy buffer paragraphs [0112], abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 8 Parolari discloses claim 1. Parolari also discloses that the IR processing module operates as a slave to the system processor (figure 5 the control processor is the master of the receiving section control that includes the IR control paragraph [0112]).

As per claim 9 Parolari discloses claim 1. Parolari also discloses that the system processor interfaces with the IR processing module via a plurality of registers (figure 5 incremental redundancy buffer paragraph [0112]); and the IR processing module

asserts an interrupt to the system processor to indicate the completion of a processing task (figure 5 incremental redundancy buffer output IRout input to the Control Processor paragraph [0112]).

As per claim 10 Parolari discloses claim 1. Parolari also discloses that the system supports Modulation and Coding Scheme (MCS) modes of the GSM EDGE standardized protocol (abstract, paragraphs [0047], [0048], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 11 Parolari discloses claim 1. Parolari also discloses IR memory including Type I IR memory and Type II IR memory, wherein control information is stored in Type I IR memory and soft decision bits are stored in Type II IR memory (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 12 Parolari discloses claim 11. Parolari also discloses punctured soft decision bits or depunctured soft decision bits may be stored in each Type II IR memory location (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 13 Parolari discloses claim 1. Parolari also discloses that the data block may include a complete Radio Link Control (RLC) block or a segmented RLC block (abstract, paragraphs [0011], [0023]-[0026], [0051]-[0052], and [0074]).

As per claim 14 Parolari discloses a system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising at least one processing device that is operable to receive an analog signal corresponding to a data block, to

sample the analog signal to produce samples, to equalize the samples, to produce soft decision bits of the data block, and to initiate IR operations (figure 5 blocks A/D, MLSE and channel decoder, paragraph [0112]); and an IR processing module coupled to the at least one processing device that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits (figure 5 block channel decoder, control processor and incremental redundancy buffer paragraph [0112]).

As per claim 15 Parolari discloses claim 14. Parolari also discloses that the processing device is operable to decode the soft decision bits to produce a decoded header for the data block (paragraphs [0024]-[0026]; paragraph [0074]; figure 4 and figure 5 paragraphs [0011] and [0112]).

As per claim 16 Parolari discloses claim 14. Parolari also discloses that the IR processing module is operable to decode the soft decision bits to produce a decoded header for the data block (paragraphs [0024]-[0026]; paragraph [0074]; figure 4 and figure 5 paragraphs [0011] and [0112]).

As per claim 18 Parolari discloses claim 14. Parolari also discloses that when the IR operations are unsuccessful, the soft decision bits of the data block are stored in IR memory (figure 5 incremental redundancy buffer paragraphs [0112], abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 21 Parolari discloses claim 14. Parolari also discloses that the IR processing module operates as a slave to the system processor (figure 5 the control processor is the master of the receiving section control that includes the IR control paragraph [0112]).

As per claim 22 Parolari discloses claim 14. Parolari also discloses that the system processor interfaces with the IR processing module via a plurality of registers (figure 5 incremental redundancy buffer paragraph [0112]); and the IR processing module asserts an interrupt to the system processor to indicate the completion of a processing task (figure 5 incremental redundancy buffer output IRout input to the Control Processor paragraph [0112]).

As per claim 23 Parolari discloses claim 14. Parolari also discloses that the system supports Modulation and Coding Scheme (MCS) modes of the GSM EDGE standardized protocol (abstract, paragraphs [0047], [0048], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 24 Parolari discloses claim 14. Parolari also discloses IR memory including Type I IR memory and Type II IR memory, wherein control information is stored in Type I IR memory and soft decision bits are stored in Type II IR memory (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 25 Parolari discloses claim 24. Parolari also discloses punctured soft decision bits or depunctured soft decision bits may be stored in each Type II IR memory location (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 26 Parolari discloses claim 14. Parolari also discloses that the data block may include a complete Radio Link Control (RLC) block or a segmented RLC block (abstract, paragraphs [0011], [0023]-[0026], [0051]-[0052], and [0074]).

As per claim 27 Parolari discloses a method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising receiving an analog signal corresponding to a data block (figure 5 antenna paragraph [0112]); sampling the analog signal to produce samples (figure 5 block A/D paragraph [0112]); equalizing the samples to produce soft decision bits of the data block (figure 5 block MLSE paragraph [0112]); transferring the soft decisions of the data block to an IR processing module (figure 5 block MLSE to channel decoder and IR buffer paragraph [0112]); and the IR processing module receiving the soft decision bits of the data block and performing IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block (figure 5 block channel decoder and IR buffer paragraph [0112]).

As per claim 30 Parolari discloses claim 27. Parolari also discloses failing to correctly decode the soft decision bits of the data block (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); storing the soft decision bits of the data block in an IR memory (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); receiving a new copy of the data block (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); determining that a Modulation and Coding Scheme (MCS) mode of the data block and a MCS mode of the new copy of the data block are compatible (abstract, paragraphs [0047], [0048], and [0074]; figure 5 paragraphs [0112] and [0113]); combining soft decision bits of the new copy of the data block with soft decision bits of the data block to produce combined soft decision bits (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); and the IR processing

module decoding the combined soft decision bits (figure 5 block channel decoder and IR buffer paragraph [0112]).

As per claim 31 Parolari discloses claim 30. Parolari also discloses failing to correctly decode the combined soft decision bits (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); and storing the combined soft decision bits in an IR memory (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 32 Parolari discloses claim 30. Parolari also discloses combining soft decision bits of the new copy of the data block with soft decision bits of the data block to produce combined soft decision bits comprises combining punctured soft decision bits when a MCS mode of the data block is the same as a MCS mode of the new copy of the data block (paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); and a puncturing pattern of the data block is the same as a puncturing pattern of the new copy of the data block (paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]).

As per claim 34 Parolari discloses claim 27. Parolari also discloses each symbol of the data block is represented by four punctured soft decision bits; and each symbol of the data block is also represented by five depunctured soft decision bits (paragraph [0074] and tables 1-4)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6, 7, 17, 19, 20, 28, 29 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parolari as applied to claim 1 above, and further in view of Ramesh (US 6909758 B2).

As per claim 4 Parolari discloses claim 1. Parolari also discloses a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block is determined (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]); the soft decision bits are deinterleaved (figure 5 block de-interleaver paragraphs [0074] and [0112]). Parolari doesn't specifically disclose the inherently process that the soft decision bits are depunctured to produce depunctured soft decision bits; and the IR processing module is operable to decode the depunctured soft decision bits. Ramesh discloses that the soft decision bits are depunctured to produce depunctured soft decision bits (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and the IR processing module is operable to decode the depunctured soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5 block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it

would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 4.

As per claim 6 Parolari discloses claim 5. Parolari also discloses that in a subsequently received copy of the data block a determination is made that a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the subsequently received copy of the data block and a MCS mode of the data block are compatible (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]); soft decision bits of the subsequently received copy of the data block are combined with soft decision bits of the data block to produce combined soft decision bits (figure 5 block channel decoder, control processor and incremental redundancy buffer paragraph [0112]). Parolari doesn't specifically disclose the inherently process that the combined soft decision bits are depunctured; and the IR processing module decodes the depunctured combined soft decision bits. Ramesh discloses that the combined soft decision bits are depunctured (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and the IR processing module decodes the depunctured combined soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5 block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it

would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 6.

As per claim 7 Parolari discloses claim 5. Parolari also discloses that in a subsequently received copy of the data block: a determination is made that a Modulation and Coding Scheme (MCS) mode of the subsequently received copy of the data block and a MCS mode and puncturing pattern of the data block are compatible (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]); the soft decision bits of the data block produce first soft decision bits (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); the soft decision bits of data of the subsequently received copy of the data block produce second soft decision bits (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); the first soft decision bits and the second soft decision bits are combined to produce combined soft decision bits (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); and the IR processing module is operable to decode the combined soft decision bits (abstract figure 5 channel decoder paragraphs [0051] and [0112] type II IR). Parolari doesn't specifically disclose the inherently process that the combined soft decision bits are depunctured; and the IR processing module decodes the depunctured combined soft decision bits. Ramesh discloses that the combined soft decision bits are depunctured (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and the IR processing module decodes the depunctured combined soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5 block 580 column 8 lines 23-36). Parolari and

Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 7.

As per claim 17 Parolari discloses claim 14. Parolari also discloses a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block is determined (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]). Parolari doesn't specifically disclose the inherently process that the soft decision bits are depunctured to produce depunctured soft decision bits; and the IR processing module is operable to decode the depunctured soft decision bits. Ramesh discloses that the soft decision bits are depunctured to produce depunctured soft decision bits (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and the IR processing module is operable to decode the depunctured soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5 block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to

depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 17.

As per claim 19 Parolari discloses claim 18. Parolari also discloses that in a subsequently received copy of the data block a determination is made that a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the subsequently received copy of the data block and a MCS mode of the data block are compatible (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]); soft decision bits of the subsequently received copy of the data block are combined with soft decision bits of the data block to produce combined soft decision bits (figure 5 block channel decoder, control processor and incremental redundancy buffer paragraph [0112]). Parolari doesn't specifically disclose the inherently process that the combined soft decision bits are depunctured; and the IR processing module decodes the depunctured combined soft decision bits. Ramesh discloses that the combined soft decision bits are depunctured (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and the IR processing module decodes the depunctured combined soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5 block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been

to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 19.

As per claim 20 Parolari discloses claim 18. Parolari also discloses that in a subsequently received copy of the data block: a determination is made that a Modulation and Coding Scheme (MCS) mode of the subsequently received copy of the data block and a MCS mode and puncturing pattern of the data block are compatible (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]); the soft decision bits of the data block produce first soft decision bits (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); the soft decision bits of data of the subsequently received copy of the data block produce second soft decision bits (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); the first soft decision bits and the second soft decision bits are combined to produce combined soft decision bits (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); and the IR processing module is operable to decode the combined soft decision bits (abstract figure 5 channel decoder paragraphs [0051] and [0112] type II IR). Parolari doesn't specifically disclose the inherently process that the combined soft decision bits are depunctured; and the IR processing module decodes the depunctured combined soft decision bits. Ramesh discloses that the combined soft decision bits are depunctured (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and decoding the depunctured combined soft decision bits (figure 2 block 240 column 4 lines 22-34 and

figure 5 block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 20.

As per claim 28 Parolari discloses claim 27. Parolari also discloses decoding the soft decision bits of the data block to produce a decoded header (paragraphs [0024]-[0026]; paragraph [0074]; figure 4 and figure 5 paragraphs [0011] and [0112]); and determining a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header (figure 5 control processor and MOD-TX-SEL paragraphs [0074] and [0112] and figure 16 block S2 paragraphs [0137] and [0162]). Parolari doesn't specifically disclose the inherently process of depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and decoding the depunctured soft decision bits. Ramesh discloses depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and decoding the depunctured soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5 block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would

have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 28.

As per claim 29 Parolari and Ramesh discloses claim 28. Ramesh also discloses that the IR processing module performs the depuncturing operations (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 29.

As per claim 33 Parolari discloses claim 30. Parolari doesn't specifically disclose the inherently process of depuncturing the soft decision bits of the data block to produce first depunctured soft decision bits; depuncturing the soft decision bits of the new copy of the data block to produce second depunctured soft decision bits; and combining the first depunctured soft decision bits with the second depunctured soft decision bits to produce the combined soft decision bits. Ramesh discloses depuncturing the soft decision bits of the data block to produce first depunctured soft decision bits (figure 2

block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); depuncturing the soft decision bits of the new copy of the data block to produce second depunctured soft decision bits (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and combining the first depunctured soft decision bits with the second depunctured soft decision bits to produce the combined soft decision bits (figure 2 block 240 column 5 lines 41-51 and figure 5 block 520 column 7 lines 32-49). Parolari and Ramesh are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the decoding technique disclosed by Ramesh in the link adaptation system disclosed by Parolari. The suggestion/motivation for doing so would have been to depuncturing a punctured data block (Ramesh column 4 lines 30-34). Therefore, it would have been obvious to combine Parolari and Ramesh to obtain the invention as specified in claim 33.

Double Patenting

Claims 1, 6, 7, 14, 27, 28 and 34 of this application, conflict with claims 1, 12, 27, 16, 1, 12, and 31 respectively of Application No. 10/791,945. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 6, 7, 14, 27, 28 and 34 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 12, 27, 16, 1, 12, and 31 respectively of copending Application No. 10/791,945. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims are substantially the same.

As per claims 1 (10/731803) and 1 (10/791945) application with serial No. 10/731803 claims "A system for implementing Incremental Redundancy (IR) operations

in a wireless receiver comprising: a baseband processor that is operable to receive analog signals corresponding to a data block and to sample the analog signal to produce samples; an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block; a system processor that is operable to receive the soft decision bits and to initiate IR operations; and an IR processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits" and application with serial No. 10/791945 claims "A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising: receiving an analog signal corresponding to a data block; sampling the analog signal to produce samples; equalizing the samples to produce soft decision bits of the data block; configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers; initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and accessing, by the IR processing module, the plurality of IR processing module registers; and performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block". It is obvious that both applications claim essentially the same limitations, receiving, sampling, equalizing, IR processing (initialization and accessing is inherent to processing).

As per claim 6 (10/731803) and 12 (10/791945), application with serial No. 10/731803 claims "the soft decision bits of the data block are stored in IR memory; a determination is made that a Modulation and Coding Scheme (MCS) mode and

puncturing pattern of the subsequently received copy of the data block and a MCS mode of the data block are compatible; soft decision bits of the subsequently received copy of the data block are combined with soft decision bits of the data block to produce combined soft decision bits; the combined soft decision bits are depunctured; and the IR processing module decodes the depunctured combined soft decision bits" and application with serial No. 10/791945 claims "decoding the soft decision bits of the data block to produce a decoded header; and identifying a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header; depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and decoding the depunctured soft decision bits". It is obvious that both applications claim the same limitations, identify modulation, depuncture, and decoding.

As per claims 7 (10/731803) and 27 (10/791945), application with serial No. 10/731803 claims "a determination is made that a Modulation and Coding Scheme (MCS) mode of the subsequently received copy of the data block and a MCS mode and puncturing pattern of the data block are compatible; the soft decision bits of the data block are depunctured to produce first depunctured soft decision bits; the soft decision bits of data of the subsequently received copy of the data block are depunctured to produce second depunctured soft decision bits; the first depunctured soft decision bits and the second depunctured soft decision bits are combined to produce combined depunctured soft decision bits; and the IR processing module is operable to decode the combined depunctured soft decision bits." and application with serial No. 10/791945

claims "decode the soft decision bits of the data block to produce a decoded header; and identify a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header; depuncture the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and decode the depunctured soft decision bits". It is obvious that both applications claim the same limitations, identify modulation, depuncture, and decoding.

As per claims 14 (10/731803) and 16 (10/791945), application with serial No. 10/731803 claims "A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising: at least one processing device that is operable to receive an analog signal corresponding to a data block, to sample the analog signal to produce samples, to equalize the samples, to produce soft decision bits of the data block, and to initiate IR operations; and an IR processing module operably coupled to the at least one processing device that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits" and application with serial No. 10/791945 claims "A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising: a baseband processor that is operable to receive analog signals corresponding to a data block and to produce samples of the analog signals; an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block; a system processor that is operable to receive the soft decision bits of the data block; a plurality of IR processing module registers communicatively coupled to the system processor; an IR processing module communicatively coupled to the system processor

and to the plurality of IR processing module registers; wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block". It is obvious that both applications claim essentially the same limitations, receiving, sampling, equalizing, IR processing (initialization and accessing is inherent to processing).

As per claims 27 (10/731803) and 1 (10/791945) application with serial No. 10/731803 claims "A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising: receiving an analog signal corresponding to a data block; sampling the analog signal to produce samples; equalizing the samples to produce soft decision bits of the data block; transferring the soft decisions of the data block to an IR processing module; and the IR processing module receiving the soft decision bits of the data block and performing IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block" and application with serial No. 10/791945 claims "A method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising: receiving an analog signal corresponding to a data block; sampling the analog signal to produce samples; equalizing the samples to produce soft decision bits of the data block; configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers; initiating, by the system

processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and accessing, by the IR processing module, the plurality of IR processing module registers; and performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block". It is obvious that both applications claim essentially the same limitations, receiving, sampling, equalizing, IR processing (initialization and accessing is inherent to processing).

As per claims 28 (10/731803) and 12 (10/791945) application with serial No. 10/731803 claims "decoding the soft decision bits of the data block to produce a decoded header; and determining a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header; depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and the IR processing module decoding the depunctured soft decision bits" and application with serial No. 10/791945 claims "decoding the soft decision bits of the data block to produce a decoded header; and identifying a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header; depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and decoding the depunctured soft decision bits". It is obvious that both applications claim the same limitations, identify modulation, depuncture, and decoding.

As per claims 34 (10/731803) and 31 (10/791945) application with serial No. 10/731803 claims "each symbol of the data block is represented by four punctured soft

decision bits; and each symbol of the data block is also represented by five depunctured soft decision bits" and application with serial No. 10/791945 claims "each symbol of the data block is represented by four punctured soft decision bits; and each symbol of the data block is also represented by five depunctured soft decision bits". It is obvious that both applications claim the same limitations, identify modulation, depuncture, and decoding. It is obvious that both applications claim the same limitations.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Balachandran (EP 938207 A2) discloses System and method for incremental redundancy transmission in a communication system equivalent to the present application. Sipola (US 20020009157 A1) discloses a method and an apparatus implementing the method so as to enable efficient simultaneous utilization of link adaptation and incremental redundancy equivalent to the present application. Ramesh (US 20020159545 A1) discloses an incremental redundancy scheme where a transmitting device transmits an initial data block with relatively few redundancy bits, yielding a high bit rate if decoding at the receiving device is successful. If decoding fails, additional redundancy bits are transmitted until the decoding is successful, equivalent to the present application. Nobelen (US 20020099994 A1) discloses Incremental redundancy radio link protocol.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
12-12-2005

KEVIN BURD
PRIMARY EXAMINER